QUICKSWITCH® PRODUCTS LAST VALUE LATCH 20 ACTIVE BUS TERMINATORS (BUS HOLD)

IDTQS3389

FEATURES:

- Active termination pulls bus pins to rails
- Holds last value of input signal
- Ideal replacement for resistive termination
- Ultra low 3µA DC quiescent current
- Bus-hold eliminates floating bus lines and reduces static power consumption
- Low power QCMOS technology
- Operates over 2.7 to 5.5V Vcc range
- TTL-compatible input and output levels
- No added noise or ground bounce
- 20 independent terminator circuits
- Available in 24-pin QSOP package

APPLICATIONS

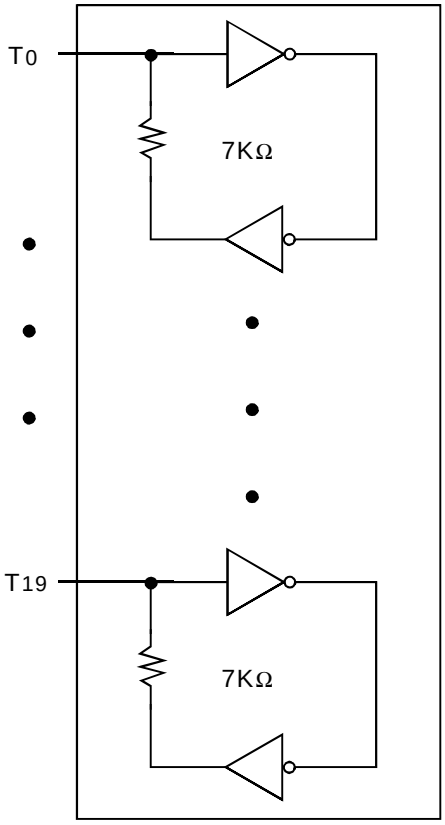
- Bus termination
- Extend data hold time

DESCRIPTION

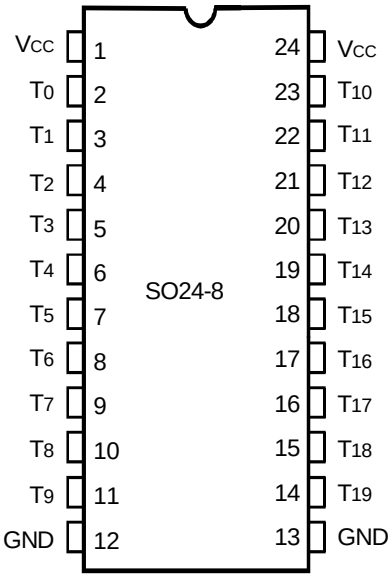
The QS3389 provides a set of 20 active termination circuits which pull data bus signals to the voltage rails. This feature prevents bus signals from floating in the threshold region of standard TTL I/O devices. The QS3389 can replace resistor termination solutions which add DC power dissipation and increase component count. Input clamp diodes help to reduce reflections and undershoot in transmission line environments. Importantly, the terminator circuits pull signals to whichever logic state the signal previously held (high or low). For this reason, this device is also referred to as a last value latch. This device is appropriate for data bus applications where interfacing devices have CMOS inputs with low input currents. These terminators provide sufficient drive to overcome leakage currents and drive corresponding signals away from the TTL threshold region.

The QS3389 is characterized for operation at 0°C to +70°C.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Description	Max.	Unit
V_{TERM}(2)	Supply Voltage to Ground	– 0.5 to +7	V
V_{TERM}(3)	DC Switch Voltage Vs	– 0.5 to +7	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	-3	V
I_{OUT}	DC Output Current	120	mA
P_{MAX}	Maximum Power Dissipation (T_A = 85°C)	.5	W
T_{STG}	Storage Temperature	– 65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc Terminals.
3. All terminals except Vcc.

CAPACITANCE

(T_A = +25°C, f = 1.0MHz, V_{IN} = 0V, V_{OUT} = 0V)

Pins	Typ.	Max. (1)	Unit
T_{19} - T_0	3	4	pF

NOTE:
1. This parameter is guaranteed at characterization but not production tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%

Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage			2	—	—	V
V_{IL}	Input LOW Voltage			—	—	0.8	V
V_T	Threshold Voltage			—	1.5	—	V
I_{IN}	Input Leakage Current (2)	V_{IN} = Vcc or GND		—	—	±5	µA
I_{BH}	Input Current (5)	Vcc = Max., V_{IN} = 0V or Vcc		—	—	±20	µA
	Input HIGH or LOW Bus Hold Inputs (2,3)	Vcc = Max., 0.8V < V_{IN} < 2V		—	—	±500(4)	µA
I_{BHH}	Bus Hold Sustaining Current (6,7)	Vcc = Min.	V_{IN} = 2V	– 60	—	—	µA
I_{BHL}	Bus Hold Inputs	Vcc = Min.	V_{IN} = 0.8V	+ 60	—	—	µA
R_T	Terminator Resistance			—	7k	—	Ω

NOTES:
1. Typical values are at V_{CC} = 5.0V, T_A = 25°C.
2. Trip current definition (see Functional Block Diagram):
   An external driver must source at least I_{TL} to switch the node from LOW to HIGH.
   An external driver must sink at least I_{TH} to switch the node from HIGH to LOW.
3. Hold current definition (see Functional Block Diagram):
   I_{HH} is the Maximum Curent the QS3389 can sink without raising the node above V_{IL} max.
   I_{HL} is the Maximum Curent the QS3389 can source without lowering the node below V_{IH} min.
4. An external driver must provide at least I_{BH} during transition to guarantee that the Bus-Hold input will change states.
5. I_{BH} is the magnitude of the input current specified under two conditions:
   a) Input voltage at GND or Vcc. This indicates the input current under steady-state condition.
   b) Input voltage between 0.8V and 2V (TTL input threshold range). This indicates the maximum input current during transient condition. The driver connected to the input must overcome this current requirement in order to switch the logic state of the bus-hold circuit.
6. I_{BHL} is the minimum sustaining "sink" current at the input for V_{IN} = 0.8V. This parameter signifies the latching capability of the bus-hold circuit in logic LOW state.
7. I_{BHH} is the minimum sustaining "source" current at the input for V_{IN} = 2V. This parameter signifies the latching capability of the bus-hold circuit in logic HIGH state.

POWER SUPPLY CHARACTERISTICS

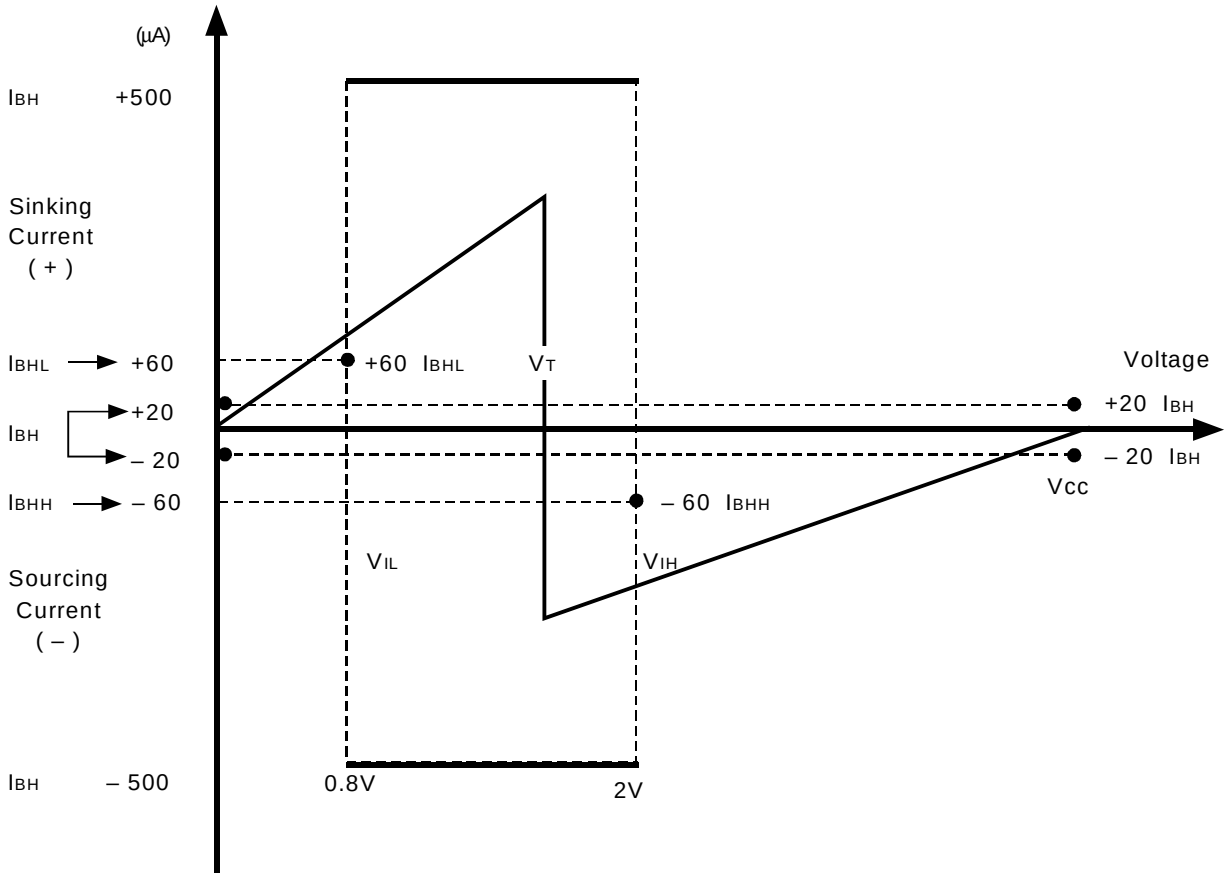
Symbol	Parameter	Test Conditions(1)	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or Vcc, f = 0	1.5	mA

NOTE:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

ACTIVE TERMINATOR OR "BUS-HOLD" CIRCUIT

The Active Terminator circuit, also known as the bus-hold circuit, is configured as a "weak latch" with positive feedback. When connected to a TTL or CMOS input port, the bus-hold circuit holds the last logic state at the input when the input is "disconnected" from the driver. When the output of a device connected to such an input attempts a logic level transition, it will overdrive the bus-hold circuit. The primary benefit of a bus-hold circuit is that it prevents CMOS inputs from floating, a situation which should be avoided to prevent spurious switching of inputs and unnecessary power dissipation. Bus-hold is a better solution than the traditional approach of using resistive termination to Vcc or GND to prevent bus floating, because the bus-hold circuit does not consume any static power.

V-I CHARACTERISTICS OF BUS-HOLD CIRCUIT

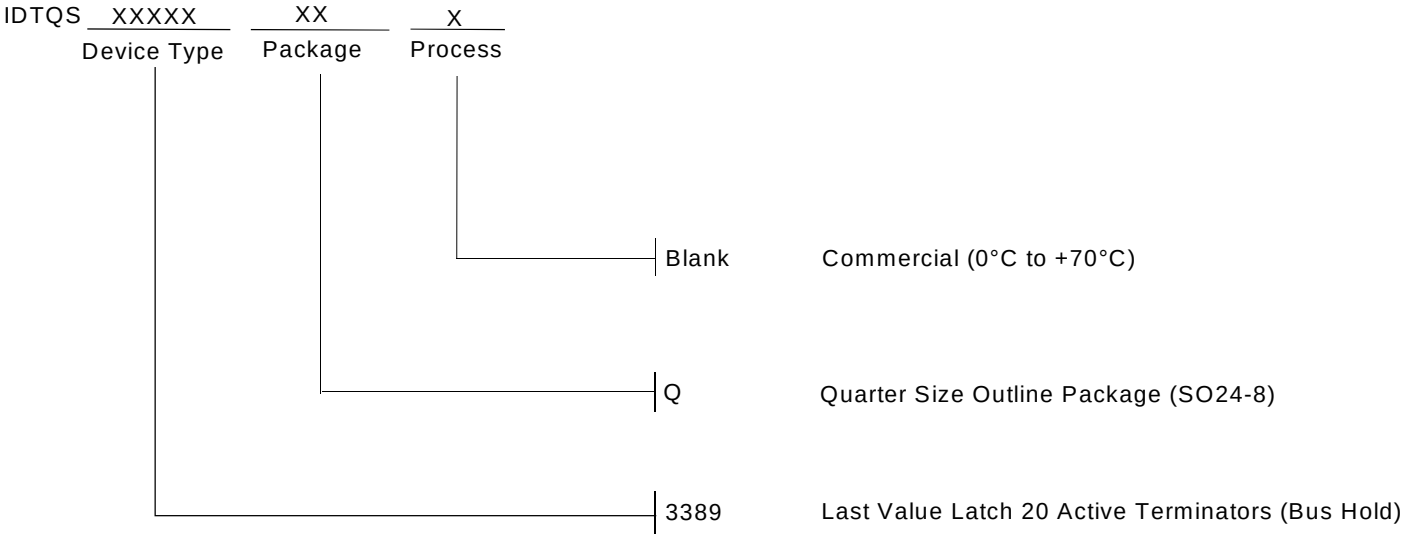


$V_T \equiv$ Threshold Voltage $\approx 1.5V$

$V_{IL} \approx .8$ $V_{IH} \approx 2V$

This figure shows the input V-I characteristics of a typical bus-hold implementation. The input characteristics resemble a resistor. As the input voltage is increased from 0 volts, the input "sink" current increases linearly. When the TTL threshold of the circuit is reached (typically 1.5 volts), the latch changes the logic state due to positive feedback and the direction of the current is reversed. As the input voltage is further increased towards Vcc, the input "source" current begins to decrease, reaching the lowest level at V_{IN} = Vcc.

ORDERING INFORMATION



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